channel stopper region.

7. (Amended) A semiconductor device according to claim 11 wherein said diffusion layer of the first conductivity type is a channel stopper region.

8. (Amended) A semiconductor device according to claim 12 wherein said diffusion layer of the first conductivity type is a channel stopper region.

Please add the following claims:

--9. A semiconductor device comprising:

a gate insulator film of a transistor formed in a predetermined region on a region of a first conductivity type;

a gate electrode of said transistor formed on said gate insulator film;

a source diffusion layer and a drain diffusion layer of a second conductivity type formed on the region of the first conductivity type;

a source side offset diffusion layer and a drain side offset diffusion layer of the second conductivity type being present around said source diffusion layer and said drain diffusion layer, respectively, so as to be in contact therewith, respectively; and

a diffusion layer of the first conductivity type formed so as to surround said source side offset diffusion layer, said drain

side offset diffusion layer and said gate insulator film so as to be in contact therewith, said diffusion layer of the first conductivity type having a higher impurity concentration than said region of the first conductivity type, and in which regions at both ends, in a direction of a channel width, of said gate insulator film protrude from a boundary, in a lateral direction, between said source side offset diffusion layer and said drain side offset diffusion layer,

wherein said diffusion layer of the first conductivity type is formed so as not to be present below said gate insulator film but to be in contact with the protruding regions at both ends, in the direction of the channel width, of said gate insulator film.

10. A semiconductor device comprising:

a gate insulator film of a transistor formed in a predetermined region on a region of a first conductivity type;

a gate electrode of said transistor formed on said gate insulator film;

a source diffusion layer and a drain diffusion layer of a second conductivity type formed on the region of the first conductivity type;

a source side offset diffusion layer and a drain side offset diffusion layer of the second conductivity type being present

around said source diffusion layer and said drain diffusion layer so as to be in contact therewith, respectively; and

a diffusion layer of the first conductivity type formed so as to surround said source side offset diffusion layer, said drain side offset diffusion layer and said gate insulator film so as to be in contact therewith, said diffusion layer of the first conductivity type having a higher impurity concentration than said region of the first conductivity type, and in which regions at both ends, in a direction of a channel width, of said gate insulator film protrude from a boundary, in a lateral direction, between said source side offset diffusion layer and said drain side offset diffusion layer,

wherein said diffusion layer of the first conductivity type is formed so as to be separate from the protruding regions at both ends, in the direction of the channel width, of said gate insulator film.

11. A semiconductor device according to claim 9, wherein said transistor is a high voltage transistor, said source diffusion layer and said drain diffusion layer are high impurity concentration, and said source side offset diffusion layer and said drain side offset diffusion layer are lower in impurity

concentration than said source diffusion layer and said drain diffusion layer.

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12. A semiconductor device according to claim 10, wherein said transistor is a high voltage transistor, said source diffusion layer and said drain diffusion layer are high impurity concentration, and said source side offset diffusion layer and said drain side offset diffusion layer are lower in impurity concentration than said source diffusion layer and said drain diffusion layer.--